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## Strategies to Reduce Power during VLSI Circuit Testing

By Kundu, Subhadip / Chattopadhyay, Santanu

Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Reduction of Dynamic and Leakage Power during Testing of Digital VLSI Circuits | Testing is now considered as one of the most important issues in the development process of integrated circuits. With the advent of deep sub-micron (DSM) technology, the tight constraints on power dissipation have created new challenges for testing low power VLSI circuits. This necessitates redesigning the traditional test techniques that do not account for power dissipation during test application. Test power is always expected to be higher than that in the normal mode of operation of a circuit. High test power may lead to permanent or temporal damage of the chip. The objective of this thesis is to develop strategies to reduce test power consumption, considering both dynamic and leakage power, without compromising the fault coverage and thus increasing the manufacturing yield. Four different strategies (three for external testing and one for internal testing) have been developed in such a way that they require either zero or very small overhead in terms of area. The techniques also have no impact on fault coverage and functional critical path | Format: Paperback | Language/Sprache: english | 116 pp.



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