

OCIN_TSIM - A DVFS AWARE SIMULATOR FOR NOC DESIGN SPACE EXPLORATION



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OCIN_TSIM - A DVFS AWARE SIMULATOR FOR NOC DESIGN SPACE EXPLORATION



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Condition: New. Publisher/Verlag: Dictus Publishing | Ocin_tsim A DVFS Aware Simulator for NoC Design Space Exploration and Optimization | Networks-on-Chip (NoCs) are a general purpose, scalable replacement for shared medium wired interconnects offering many practical applications in industry. Dynamic Voltage Frequency Scaling (DVFS) is a technique whereby a chip's voltage-frequency levels are varied at run time, often used to conserve dynamic power. Various DVFS-based NoC optimization techniques have been proposed. However, due to the resources required to validate architectural decisions through prototyping, few are implemented. As a result, designers are faced with a lack of insight into potential power savings or performance gains at early architecture stages. This thesis proposes a DVFS aware NoC simulator with support for per node power-frequency modeling and rich visualisation to allow fine-tuning of such optimization techniques early on in the design cycle. The proposed simulator also provides a framework for benchmarking various candidate strategies to allow selective prototyping and optimization. As part of the research, DVFS extensions were built for an existing NoC performance simulator and released for public use. This thesis also serves as a technical manual for the simulator extensions. | Format: Paperback | Language/Sprache: english | 76 pp.



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